NRL Report 7482

Comparative Analysis of the use of Dynamic and Static Shift Registers in Digital Signal Processors

L. M. LEIBOWITZ

Aerospace Radar Branch
Radar Division

December 26, 1972

NAVAL RESEARCH LABORATORY
Washington, D.C.

CONTENTS

ABSTRACT

High-density shift-register devices are used in many present-day data-processing systems such as radar digital signal processors. The number of bits of shift-register storage required increases with the need for greater radar range and resolution capability. The large-scale integrated (LSI) MOS circuit technology currently offers the possiblity of shift registers of tens of thousands of bits per cubic inch with average power dissipation below 200 μW per bit. These units can be implemented for dynamic or static operation with inherent higher power dissipation in the latter case, due to the additional circuitry required. The key characteristics of these implementations are the need for continuous clocking above some minimum frequency in the dynamic case and negligible power dissipation during quiescent operation in the static case. This report analyzes the relative power dissipation of dynamic and static models of complimentary MOS (CMOS) shift registers as applied to a digital-feedback-integrator signal processor for the practical case of a nonunity processing duty factor.

The concepts of shift-register multiplexing and staggering for the purpose of power-dissipation reduction are described and extensively analyzed. It is shown that in practice the amount of reduction in dissipated power is limited by the power required by the additional circuitry used to achieve multiplexing or staggering. The relative power dissipation for each of the different configurations is derived for the dynamic- and static-register models. For the models considered, the static-register configurations dissipate less power than the dynamic-register configurations, due to the recirculation required in the dynamic case. An "extended register" technique, which reduces the power dissipation of the dynamic registers, is presented and analyzed.

PROBLEM STATUS

Interim report on one phase of the NRL Problem.

AUTHORIZATION

NRL Problem R02-46

Manuscript submitted August 11, 1972.

COMPARATIVE ANALYSIS OF THE USE OF DYNAMIC AND STATIC SHIFT REGISTERS IN DIGITAL SIGNAL PROCESSORS

INTRODUCTION

Many state-of-the-art applications of digital techniques require the use of high-density data-storage mediums such as shift registers. This is particularly true with respect to radar digital signal processing, especially where digital filtering techniques are employed. In such applications, many independent signal samples must be processed and stored prior to subsequent combination with succeeding samples. Since the number of independent samples that are required to be stored at one time can be in the thousands, the number of bits stored per unit volume and the amount of average power dissipated per bit are prime considerations in the selection of a storage medium.

The most promising storage technology that offers the bit densities and power dissipation required by digital signal processing is that of large-scale integrated (LSI) MOS shift registers. At the present state of the art, MOS shift registers offer bit densities in tens of thousands of bits per cubic inch with average power dissipation below 200 μW per bit. These MOS shift registers can be configured for either a dynamic or static mode of operation. In the dynamic mode the register must be continuously clocked at a frequency above some minimum f_{min} and up to some maximum f_{max}. Static registers can be clocked over the frequency range from DC up to f_{max} and can remain indefinitely in a quiescent state in which the clock frequency is 0.

Since static registers offer all the performance characteristics of dynamic registers, with the addition of static operation, they obviously offer more flexibility in system design and implementation. The price paid for this flexibility is increased average power dissipation in the static units, when compared with the dynamic units at the same clock rates. The static registers, however, have negligible average power dissipation during quiescent operation. Since many radar digital signal-processing applications have nonunity processing duty factors that in many cases are quite low, it would seem that in these situations the low quiescent power dissipation of the static registers might more than compensate for the lower power-dissipation characteristics of the dynamic units.

It is the purpose of this report to present a general model of a digital feedback integrator (single-pole digital filter) representative of a type previously used in an actual NRL test-bed radar system and to present an analysis of the power-dissipation characteristics obtained through the use of both dynamic and static registers. Various operational configurations that can be used to reduce power dissipation will be considered. Models of typically available state-of-the-art dynamic and static registers to be used in the analysis will be described. It should be noted that although a particular processor model is considered here, the results are applicable to any processor employing shift registers with nonunity processing duty factors.

DIGITAL FEEDBACK INTEGRATOR

A single-pole digital filter has been implemented using a digital feedback integrator. This digital filter is the basis of a digital signal processor for an airborne test-bed radar system (1). Figure 1 is a block diagram of a basic digital feedback integrator. The integrator consists of a digital source presenting a time-sampled digital representation of the amplitude of the radar video, an input binary adder, a multilevel binary shift register of length equal to the number of range bins N_R to be processed, and a feedback binary multiplier. A digital sample of the radar return from each transmitted energy pulse is obtained for every range bin to be processed. The sample for a particular range bin is added to the weighted sum of all previous samples for that range bin and shifted into the register. The samples are obtained, and the resulting data are shifted at a rate f_P determined by the required range resolution, with one shift pulse for each range bin. The sums corresponding to each range bin are shifted through the register and properly weighted by a feedback factor $k < 1$. This beedback factor causes nonrecurring target-return samples to decay, thus discriminating against noise while allowing repetitive target returns to accumulate, thus effecting a low-pass filter. The feedback factor also prevents the stored value for each range bin from exceeding the word size of the integrator.

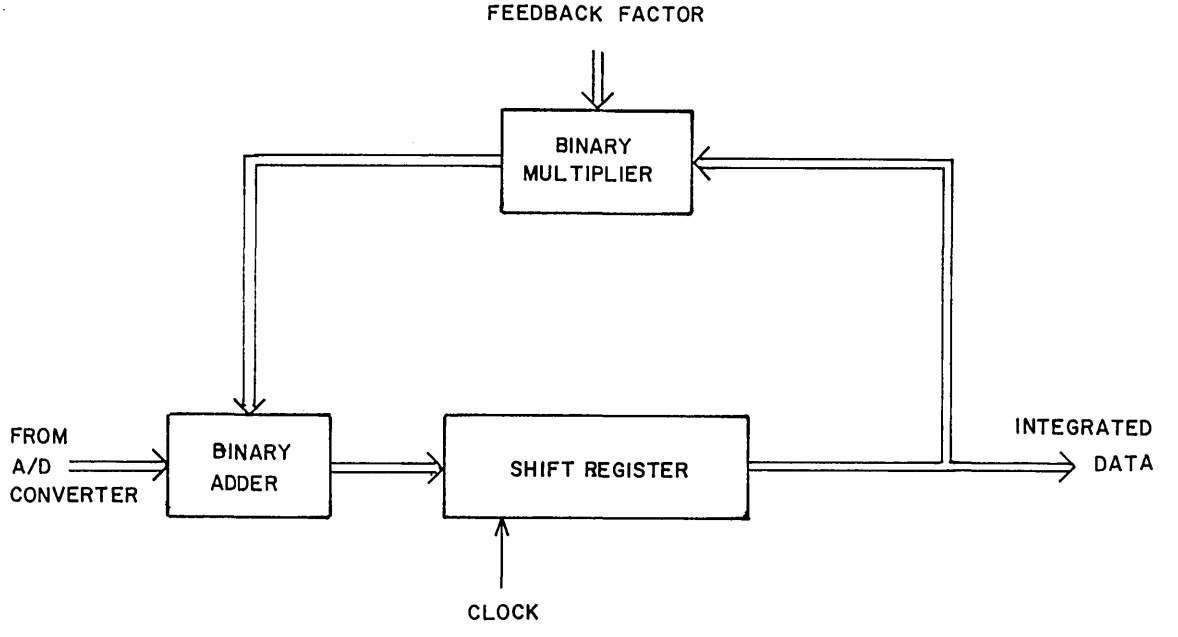

Fig. 1—Basic digital feedback integrator

In general the total range extent to be processed in the integrator determines a processing interval T_P equal to some fraction α of the total radar interpulse period T_{PRF}, where $T_{PRF} = 1/PRF$. Therefore, α is the processing duty factor. The remaining portion of T_{PRF} is defined as the data-maintenance interval T_M, which is a fraction $(1 - \alpha)$ of T_{PRF}. The processing interval T_P is determined from the number of range bins N_R processed and from the clock interval τ_R for a range bin:

$$T_P = N_R \tau_R .$$

The duty factor α can then be represented as

$$\alpha = \frac{T_P}{T_{PRF}} = \frac{N_R \tau_R}{\frac{1}{PRF}} = N_R \tau_R \cdot PRF.$$

Then the processor shift rate f_P is

$$f_P = \frac{1}{\tau_R} = \frac{N_R \cdot PRF}{\alpha}.$$

If a dynamic register were to be used to implement the integrator, the data stored in the registers following T_P would have to be recirculated during T_M by some integral multiple of N_R shift pulses, with the result that each piece of data would be back in its proper position just prior to the beginning of the succeeding PRF interval. The clock rate f_M required to recirculate the data exactly once, and thus the minimum rate required to maintain data during T_M, is thus

$$f_M = \frac{1}{\frac{T_M}{N_R}} = \frac{N_R}{T_M}.$$

However, by definition

$$T_M = T_{PRF} - T_P = \frac{1}{PRF} - N_R \tau_R,$$

and since

$$\alpha = N_R \tau_R \cdot PRF,$$

$$\frac{1}{PRF} = \frac{N_R \tau_R}{\alpha}.$$

Thus

$$T_M = \frac{N_R \tau_R}{\alpha} - N_R \tau_R = N_R \tau_R \left(\frac{1 - \alpha}{\alpha} \right).$$

Substituting $T_M = N_R / f_M$ in the above expression,

$$f_M = \frac{N_R}{N_R \tau_R \left(\frac{1 - \alpha}{\alpha} \right)} = \frac{1}{\tau_R} \left(\frac{\alpha}{1 - \alpha} \right).$$

Finally, since

$$f_P = \frac{1}{\tau_R},$$

$$f_M = \frac{\alpha}{1 - \alpha} f_P.$$

The preceding results are summarized in the timing diagram, which is Fig. 2.

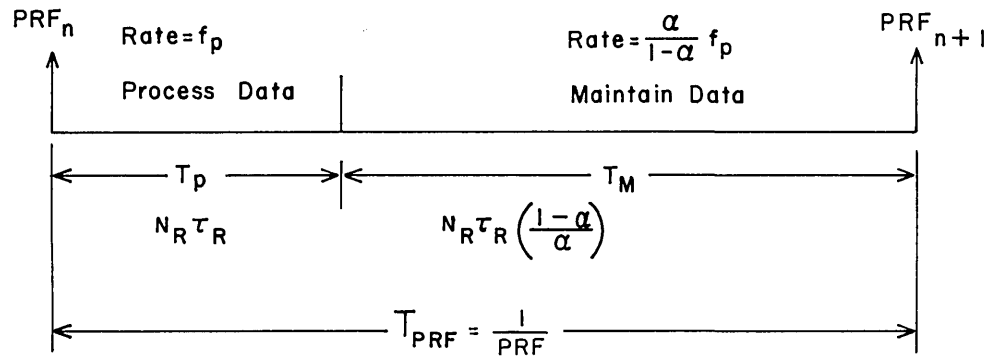

Fig. 2—Timing relationships for the data-processor model

SHIFT-REGISTER CHARACTERISTICS

At the current state of the art, the complimentary-MOS or CMOS technology seems to offer the most performance in shift registers required for digital signal processing. These devices are able to provide shift rates in excess of 10 MHz, while remaining completely compatible with the high-speed transistor-transistor logic (TTL) that must interface with these registers to achieve the required data rates in modern signal-processing applications. With these considerations, the dynamic and static shift-register models to be represented here will be based on current data on CMOS circuit techniques (2). It should be noted, however, that the basic relationships to be used here are true for the MOS technology in general, with only minor variations with specific circuitry.

Dynamic Register

As described earlier, the dynamic CMOS register is capable of clock rates over a range from some minimum f_{min} to a maximum f_{max}. The minimum frequency at which the register will be able to function is directly proportional to the gate leakage current of a particular device. For TTL-compatible operation, the typical value of f_{min} to be used for analysis can be no less than 20 kHz. Therefore, this dynamic register must be considered to be incapable of maintaining data beyond 50 μs. Thus as long as T_M is greater than 50 μs, the data in the dynamic register must be recirculated an integral number of times during T_M.

Thus, in general, recirculation is required when $T_M > 1/f_{min}$, but since $T_M = T_{PRF} - N_R\tau_R$, this is equivalent to the condition that $T_{PRF} - N_R\tau_R > 1/f_{min}$. However, $\alpha = N_R\tau_R/T_{PRF} = N_R\tau_R \cdot PRF$, and $N_R\tau_R = \alpha/PRF$. Thus

$$\frac{1}{PRF}(1-\alpha) > \frac{1}{f_{min}},$$

and finally

$$\alpha < 1 - \frac{PRF}{f_{min}}$$

is the condition under which recirculation is required when dynamic registers are used.

Each stage of the dynamic register consists of eight transistors which compose two inverters and two gates. The average power dissipated per stage is determined by the inverters, since the gate power is relatively insignificant. The power dissipation in these devices increases with frequency in a linear fashion. Thus if $P_D(f_P)$ is the average power dissipated per bit in a dynamic register at the frequency f_P, the power dissipation per bit at any frequency $f = \beta f_P$, where

$$\frac{f_{min}}{f_P} \leqslant \beta \leqslant \frac{f_{max}}{f_P},$$

is

$$P_D(\beta f_P) = \beta P_D(f_P).$$

Static Register

The static CMOS register is capable of operation at clock rates from as low as 0 (i.e., DC) up to f_{max}. Thus the static register is able to maintain stored data indefinitely without the need for recirculation and the circuitry and power dissipation associated with it. To accomplish static operation, the basic cell used in the dynamic register must be modified by the addition of an inverter or two transistors. The power dissipation in the dynamic register is due largely to the two inverters. Due to the additional inverter in the static register, the approximate relationship between P_D and P_S, the power dissipations per bit at a frequency f in the dynamic and static registers respectively is

$$P_S(f) = \frac{3}{2} P_D(f).$$

One of the most important characteristics of the CMOS static register is its extremely low power dissipation during quiescent operation at a 0 shift rate. This dissipation is due to the leakage current in the worst gate in a cell and is of the order of tens of nanowatts per bit. Thus in comparison with the power dissipation per bit at processing frequencies, which is in the range of 100 μW, the power dissipation in a static register during quiescent operation is negligible and can be considered to be 0.

SHIFT-REGISTER CONFIGURATIONS

Most digital signal processors using shift registers require overall register lengths far in excess of the length, or number of bits, available in an individual package device. To achieve these lengths, a number of basic shift-register devices of length r must be interconnected to form an overall register with length obviously equal to some integral multiple of r. There are three basic configuration techniques, serial, multiplexing, and staggering, that can be employed to accomplish this interconnection; these will be discussed here individually. Two of these techniques, multiplexing and staggering, can be used to reduce the average power dissipated in the overall shift register.

Serial

The serial interconnection configuration is shown in Fig. 3. The registers are connected in tandem with the output of each register forming the input to its succeeding register. If each basic register is of length r and if K such registers are serially interconnected, the total effective register length N_R is $N_R = K \cdot r$. The clock input is common to all registers, and thus during data processing at a frequency f_P, the power dissipated per bit is $P_D(f_P)$ or $P_S(f_P)$, depending on whether dynamic or static registers are used.

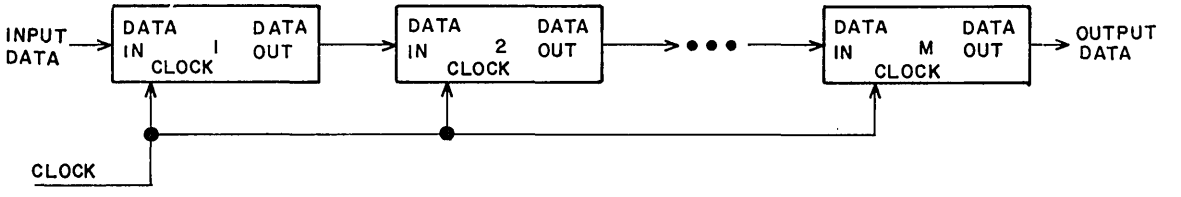

Fig. 3—Serial shift-register configuration

Multiplexed

The multiplexed configuration shown in Fig. 4, sequentially assigns each succeeding input data word to M different registers, where M is defined as the multiplex factor. To simplify the representation, logic AND gates are indicated; it is assumed that the output gates are capable of wired OR operation; gate propagation delays are ignored. Each of the

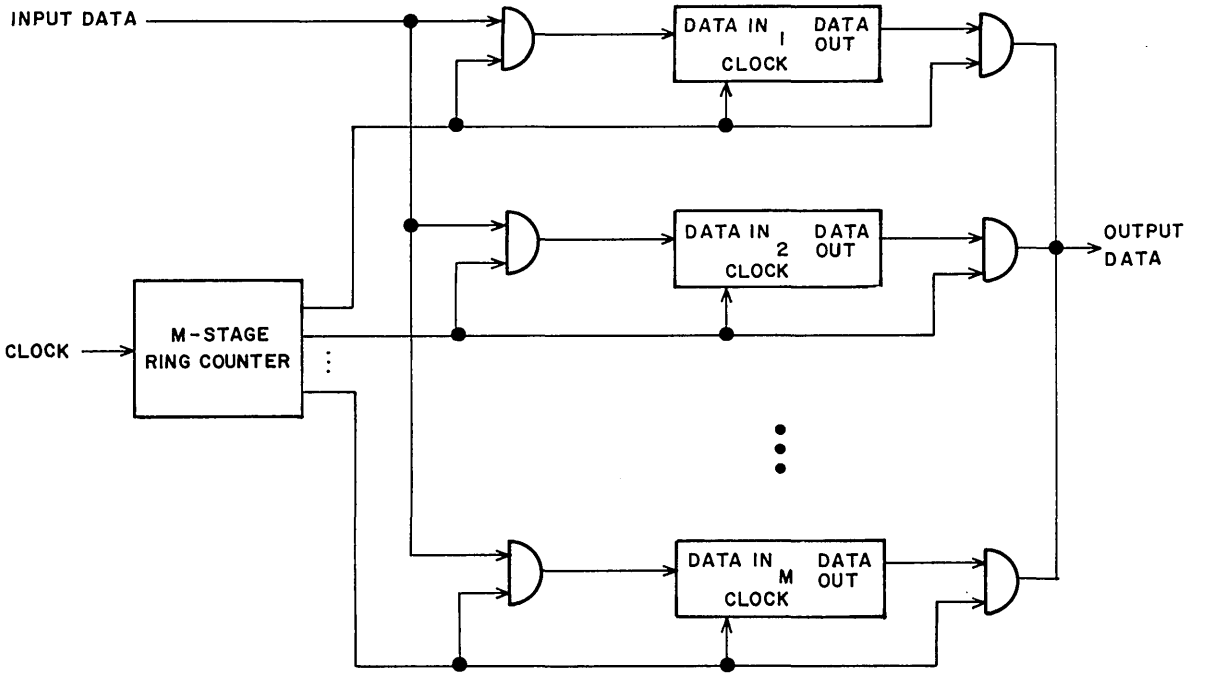

Fig. 4—Multiplexed shift-register configuration

multiplexed registers can be composed of a multiple of series-interconnected registers. If each multiplexed register is of length r, the total effective register length is $N_R = M \cdot r$.

Since each multiplexed register level receives only every Mth data word, it is clocked at a rate which is $1/M$ of the overall processing rate f_P. To form the proper clock for each of these multiplexed registers, the input clock is used to trigger an M-stage ring counter, and the output of each counter stage forms the clock input to each level of multiplexing.

Since the shift-register models as described earlier obey a linear relation between power dissipation and frequency, during processing at the effective rate f_P,

$$P_D\left(\frac{f_P}{M}\right) = \frac{P_D(f_P)}{M} .$$

Thus the power dissipation per bit using multiplexing is reduced by the multiplex factor M. This is true independent of whether dynamic or static registers are used, although multiplexing would generally be associated with dynamic registers, and the preceding relation is valid with P_D replaced by P_S.

From Fig. 4 it can be seen that to accomplish the reduction in power dissipation per bit with multiplexing, as compared to the serial configuration, an M-stage ring counter and two gates per level of multiplexing must be provided. Since this additional circuitry will also dissipate power, there is a point above which the additional power dissipated will exceed that saved through the use of multiplexing. There is an optimum value of M at which the difference between the power dissipated without multiplexing and that dissipated with multiplexing is a maximum. If P_R is the total power dissipated in the serial register, then at frequency f_P

$$P_R = N_R P_D(f_P),$$

where N_R is the total number of register bits and $P_D(f_P)$ is the power dissipation per bit at f_P. If P_m is the total power dissipated in the multiplexed register and P_G and P_{RC} are the power dissipations per level of multiplexing for each logic gate and the ring counter respectively,

$$P_m = \frac{N_R P_D(f_P)}{M} + M(2P_G + P_{RC}).$$

The difference in shift-register power dissipation with and without multiplexing is

$$P_R - P_m = N_R P_D(f_P) - \frac{N_R P_D(f_P)}{M} - M(2P_G + P_{RC}).$$

Differentiating with respect to M and setting the derivative equal to 0,

$$\frac{N_R P_D(f_P)}{M_{\text{opt}}^2} - (2P_G + P_{RC}) = 0,$$

where M_{opt} is the optimum value of M. Solving for M_{opt},

$$M_{opt} = \sqrt{\frac{N_R P_D(f_P)}{2P_G + P_{RC}}} \ .$$

Using some typical circuit-dissipation values with a register whose length N_R is 50 X 10^3, M_{opt} is approximately 20.

The above analysis is not meant to be all inclusive but is intended to show that there is an optimum value of M and to give some indication of its order of magnitude.

Staggered

Figure 5 is a block diagram of the staggered configuration. This configuration uses the ability of the static register to maintain data without dissipation of power and thus in its basic form cannot use dynamic registers. Each group of r successive data words is clocked into a staggered subregister of length r. The next group of r data words is clocked into a succeeding register of length r and so on. The number of staggered subregisters is the stagger factor S. Thus the overall register length is $N_R = S \cdot r$. Only that particular subregister receiving data words is being clocked and is dissipating power at any one instant of time; the others are in their quiescent state, maintaining data. Thus, although each register, when processing, is operating at f_P and dissipating full processing power per bit, it operates with a duty factor of $1/S$ of that in a serial register of length N_R.

Referring to the block diagram (Fig. 5), the input clock frequency f_P is divided by r, providing a clock of rate f_P/r which triggers an S-stage ring counter. Each stage of the

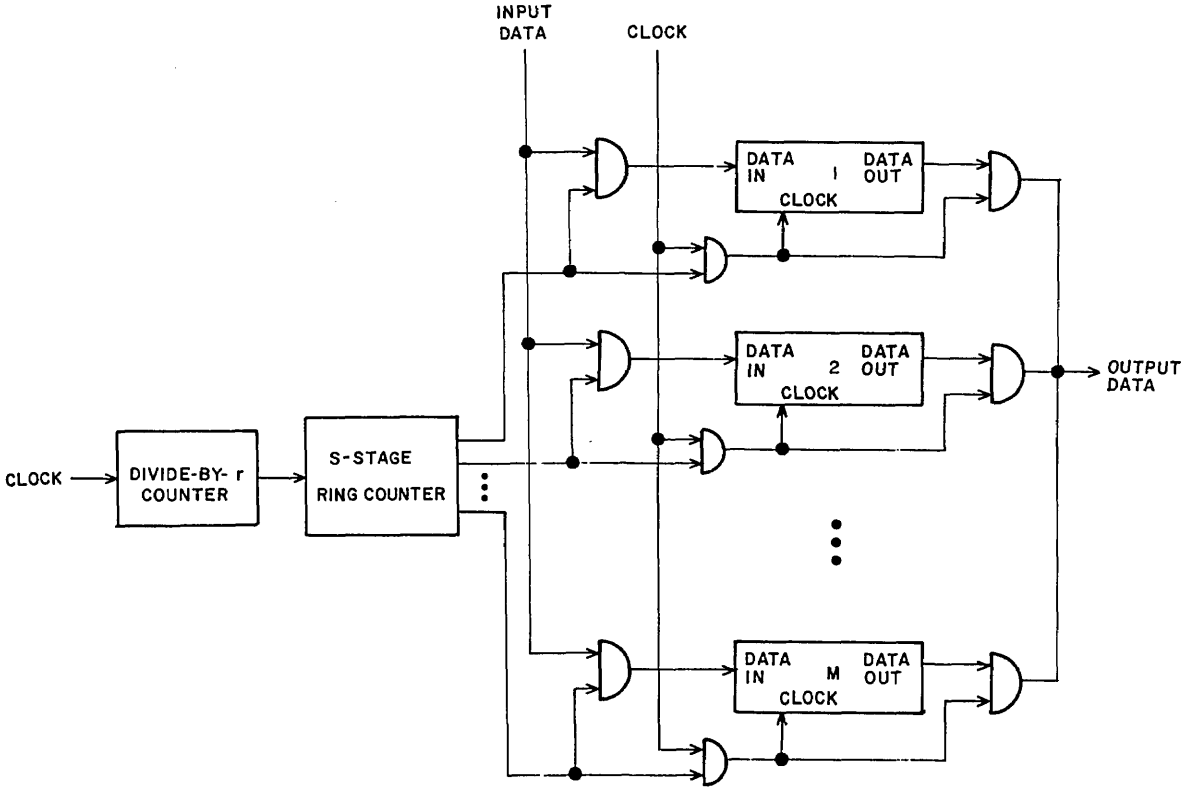

Fig. 5—Staggered shift-register configuration

ring counter provides an enable pulse to each staggered subregister. This enable pulse is of width r/f_P and occurs at a rate of f_P/N_R. This pulse occurs at only one subregister at a time and enables the data-in and clock lines to that subregister. This permits r data words, with their corresponding clock pulses, to enter a particular subregister while all other subregisters are disabled. By AND-gating the output of each subregister with its corresponding clock and combining the gated outputs from all subregisters by a wired OR operation, the output of the overall register is formed.

It can be seen that to accomplish staggering and thus reduce overall register power, one requires three gates and a ring-counter stage per staggered subregister and an r-stage counter for the overall register. The power required per level of staggering is dependent on the power dissipation per gate P_G, on the power required per ring-counter stage P_{RC}, and on some fraction of the power dissipated by the divide-by-r counter. The number of counter stages C is the lowest integral number such that $C \geqslant \log_2 r$. To simplify the analysis, it will be assumed that C varies continuously with r: $C = \log_2 r$. If P_C is the power dissipated per stage by the divide-by-r counter, then the counter power per stagger level, P_{CS}, is

$$P_{CS} = \frac{P_C \log_2 r}{S},$$

but since $N_R = S \cdot r$,

$$P_{CS} = \frac{P_C \log_2 \frac{N_R}{S}}{S}.$$

The total power P_{ST} for the staggered register is then

$$P_{ST} = \frac{N_R P_S(f_P)}{S} + S\left(3P_G + P_{RC} + \frac{P_C}{S} \log_2 \frac{N_R}{S}\right).$$

As in the case of multiplexing, it is desired to maximize the difference in power dissipation with and without staggering for a register of length N_R. Thus

$$P_R - P_{ST} = N_R P_S(f_P) - \frac{N_R P_S(f_P)}{S} - S\left(3P_G + P_{RC} + \frac{P_C}{S} \log_2 \frac{N_R}{S}\right).$$

Differentiating with respect to M and setting the derivative equal to 0,

$$\frac{N_R P_S(f_P)}{S_{opt}^2} - (3P_G + P_{RC}) + \frac{P_C}{S_{opt} \ln 2} = 0,$$

where S_{opt} is the optimum value of S, and

$$(3P_G + P_{RC}) S_{opt}^2 - \frac{P_C}{\ln 2} S_{opt} - N_R P_S(f_P) = 0.$$

Thus

$$S_{opt} = \frac{\frac{P_C}{2 \ln 2} + \sqrt{\left(\frac{P_C}{2 \ln 2}\right)^2 + (3P_G + P_{RC})(N_R P_S(f_P)}}{3P_G + P_{RC}} .$$

In a practical case, P_C, P_G, and P_{RC} are of the same order of magnitude, with $N_R P_S(f_P)$ several orders of magnitude greater for $N_R > 5000$. Under these conditions

$$(3P_G + P_{RC})N_R P_S(f_P) >> \left(\frac{P_C}{2 \ln 2}\right)$$

and

$$S_{opt} = \sqrt{\frac{N_R P_S(f_P)}{3P_G + P_{RC}}} .$$

It can be seen that S_{opt} will be slightly less than M_{opt}, due to the extra gate required at each stagger level.

COMPARATIVE POWER DISSIPATION

The signal-processor and shift-register models developed earlier will now be used to perform a comparative analysis of power dissipation per bit for the various configurations. This analysis will assume a processing frequency f_P and a duty factor α and will be performed both for dynamic and static registers. In general the total power dissipation is the sum of the power dissipated during the process-data interval and that dissipated during the maintain-data interval; these power dissipations will be referred to as P_D and P_M respectively. The power dissipation per bit for the dynamic register at the processing frequency f_P was defined to be $P_D(f_P)$. All power dissipations for the various configurations, for dynamic- and static-register use, will be found in terms of this quantity. The additional power dissipation of the logic circuitry required for multiplexing and staggering as described earlier will be neglected in this analysis.

Using dynamic registers in the serial configuration,

$$P_P = P_D(f_P)$$

and

$$P_M = P_D(f_M),$$

where f_M is the data-maintenance frequency. However, as shown previously,

$$f_M = \frac{\alpha}{1 - \alpha} f_P,$$

and therefore

$$P_M = \frac{\alpha}{1 - \alpha} P_D(f_P).$$

The total power dissipation per bit, P, is then the sum of P_P and P_M, each weighted by the fraction of the P_{PRF} interval used for data processing and maintenance respectively. Therefore

$$P = \alpha P_P + (1 - \alpha) P_M$$

Thus

$$P = \alpha P_D(f_P) + (1 - \alpha) \frac{\alpha}{1 - \alpha} P_D(f_P) = 2\alpha P_D(f_P).$$

For the multiplexed configuration, this total dissipation per bit, P, must be reduced by the multiplex factor M and is thus $2\alpha P_D(f_P)/M$. Likewise, for the staggered-register configuration, the total dissipation per bit is $2\alpha P_D(f_P)/S$.

In the case of static-register use, the maintenance power dissipation is negligible, as described earlier, but the basic dissipation per bit is 1.5 times that of the dynamic register. Thus for the serial configuration,

$$P_P = 1.5 P_D(f_P)$$

and

$$P = 1.5\alpha P_D(f_P).$$

The dissipation per bit for the multiplexed register is then $1.5\alpha P_D(f_P)/M$, and for the staggered register it is $1.5\alpha P_D(f_P)/S$. These results are summarized in Table 1.

Table 1
Power Dissipation For Various Configurations

Static Registers	P_D	P_M	P
Serial	$1.5P_D(f_P)$	0	$1.5\alpha P_D(f_P)$
Multiplexed	$\frac{1.5P_D(f_P)}{M}$	0	$\frac{1.5\alpha P_D(f_P)}{M}$
Staggered	$\frac{1.5P_D(f_P)}{S}$	0	$\frac{1.5\alpha P_D(f_P)}{S}$
Dynamic Registers			
Serial	$P_D(f_P)$	$\frac{\alpha}{1-\alpha} P_D(f_P)$	$2\alpha P_D(f_P)$
Multiplexed	$\frac{P_D(f_P)}{M}$	$\frac{\alpha}{1-\alpha} \frac{P_D(f_P)}{M}$	$\frac{2\alpha P_D(f_P)}{M}$
Staggered	$\frac{P_D(f_P)}{S}$	$\frac{\alpha}{1-\alpha} \frac{P_D(f_P)}{S}$	$\frac{2\alpha P_D(f_P)}{S}$

EXTENDED REGISTER

The basic serial-register configuration can be modified to permit use of dynamic registers in applications having a nonunity processing duty factor with little increase in power dissipation over the case of unity duty factor. This can be accomplished by an interesting technique which will be referred to here as an extended register.* The basic principle of the extended register is to provide an overall register of length $N_R + N_M$ for the serial configuration. As defined previously, N_R is the number of range bins to be processed and is the required overall length of the registers considered in our earlier analysis. The additional register positions or maintenance cells N_M must be equal to or greater than the time remaining in the *PRF* interval after N_R range bins are processed, divided by the maximum maintenance interval $1/f_{\min}$ of the dynamic register. Thus after processing N_R range bins at a rate f_P, N_M additional clock pulses at the rate $f_{\min}$ would be provided to preserve the data until the beginning of the next *PRF* interval. At that time the data would be justified to the end of the register and ready for processing in the new *PRF* interval.

The value of N_M as previously described is

$$N_M = \frac{T_M}{\frac{1}{f_{\min}}}.$$

Since it was shown previously that

$$T_M = N_R \tau_R \left(\frac{1-\alpha}{\alpha}\right)$$

and $\tau_R = 1/f_P$, it follows that

$$N_M = N_R \frac{f_{\min}}{f_P} \left(\frac{1-\alpha}{\alpha}\right).$$

The total power dissipated per required register bit is then

$$P = \alpha P_P + (1-\alpha) P_M,$$

where, if

$$\eta = \frac{f_P}{f_{\min}},$$

it follows that

*This technique was first suggested to the author in a conversation with Dr. H. L. Groginsky of the Raytheon Company Equipment Development Laboratories, Wayland, Massachusetts.

$$P_P = \frac{N_R + N_M}{N_R} P_D(f_P)$$

$$= \left[1 + \frac{f_{\min}}{f_P}\left(\frac{1-\alpha}{\alpha}\right)\right] P_D(f_P)$$

$$= \left(1 + \frac{1-\alpha}{\alpha\eta}\right) P_D(f_P)$$

and

$$P_M = \frac{N_R + N_M}{N_R} P(f_{\min})$$

$$= \left[1 + \frac{f_{\min}}{f_P}\left(\frac{1-\alpha}{\alpha}\right)\right] P_D(f_{\min})$$

$$= \left(1 + \frac{1-\alpha}{\alpha\eta}\right) \frac{P_D(f_P)}{\eta} .$$

Thus

$$P = \left(1 + \frac{1-\alpha}{\alpha\eta}\right)\left(\alpha + \frac{1-\alpha}{\eta}\right) P_D(f_P)$$

$$= \left(1 + \frac{1-\alpha}{\alpha\eta}\right)^2 \alpha P_D(f_P).$$

Since η would typically be in excess of 200 for duty factors $\alpha > 0.1$,

$$P = \alpha P_D(f_P),$$

which is basically the power per bit dissipated during the processing interval. For very small duty factors ($\alpha < 0.001$), the number of maintenance cells is inversely proportional to α. The resulting power dissipation is then

$$P = \frac{1}{(\alpha\eta)^2} \alpha P_D(f_P),$$

which will increase rapidly, in comparison with $\alpha P_D(f_P)$, as the duty factor is decreased. As an example, the radar signal processor described in Ref. 1 has a processing duty factor of $\alpha = 0.005$ at the lower *PRF* rate. Assuming $\eta = 500$, it is found that the total power per required register bit is $P = 1.95\alpha P_D(f_P)$. The power dissipation using the extended register under these conditions would then be somewhat greater than that with static registers used in a serial configuration.

If the extended-register technique is applied to a multiplexed-register or staggered-register configuration, each subregister must possess N_M additional cells. This would involve $M \cdot N_M$ additional cells in the multiplexed case and $S \cdot N_M$ in the staggered case. This would require quite a large amount of additional power in the case where α is small and

the total number of additional cells approaches the order of N_R. Due to the extreme complexity of the required clocking, it would not be desirable to apply the extended-register technique simultaneously with multiplexing or staggering.

CONCLUSIONS

This report has presented an analysis of state-of-the-art LSI dynamic and static shift registers with respect to their general characteristics and the configurations in which they might be used in digital signal-processing applications. State-of-the-art models of MOS shift registers were developed. These models were assumed to dissipate power in direct proportion to clock frequency. The static register was assumed to dissipate 1.5 times the power of the dynamic register during normal operation and negligible power during quiescent operation. The dynamic register was assumed to have a minimum clock frequency of about two orders of magnitude below the effective processing frequency.

The analysis leads to several interesting results. First, where continuous processing situations ($\alpha = 1$) exist, the dynamic register offers advantages in reduced power dissipation, due to a reduction in the number of required elements per cell. This also leads to increased bit densities per package for the dynamic register. In this continuous processing case, the register clocking requirements are straightforward and identical for both dynamic and static registers.

In the general case of nonunity processing duty factors, where the number of shift-register cells is some N_R, as required for processing, there are several interesting results. For dynamic registers with recirculation used for data maintenance, or data refreshing, the power dissipation per bit during maintenance equals that during processing. Although the dynamic register might characteristically dissipate about 2/3 the power of a static register during continuous operation, for an application having a nonunity processing duty factor, the static register dissipates 3/4 of the total power per bit of the dynamic register. This is due to the negligible power-dissipation characteristic of the static register during quiescent or nonprocessing operation. The use of techniques such as multiplexing and staggering reduce power dissipation but at the expense of more complicated clocking requirements. Multiplexing reduces power dissipation by reducing the register clock rates; staggering reduces the duty factor of each individual subregister segment of the overall register.

The extended-register technique greatly improves the power-dissipation characteristics of the dynamic register. This technique provides additional maintenance cells through which the data can be clocked at minimum rates until the following processing interval. For values of α greater than 0.1, the total power dissipation per required processing cell is essentially that dissipated during the processing interval. For very small processing duty factors, the number of maintenance cells and thus the power dissipation increase inversely with the duty factor. If multiplexing or staggering is applied to the extended-register technique, each subregister must possess the required number of maintenance cells. The total number of additional cells can then easily approach the order of the basic processing cells, with a large accompanying increase in power dissipation. The clocking requirements of a multiplexed or staggered extended register are quite complex.

ACKNOWLEDGMENTS

The author acknowledges the efforts of Mr. R. K. Baldauf, who derived many of the frequency and time relationships for the digital signal-processor model. He thanks Mrs. S. Cohee and Mrs. B. McDonald for the preparation and typing of the manuscript.

REFERENCES

1. R.K. Baldauf and L.M. Leibowitz, "Digital Signal Processor For A Test-Bed Ocean-Surveillance Radar," NRL Report 7317 (Secret Report, Unclassified Title), Aug. 26, 1971.

2. A.C. Ipri, K.M. Schlesier et al., "Advanced CMOS Circuit Techniques," Technical Report AFAL-TR-72-1, Jan. 1972, prepared by RCA Laboratories for the Air Force Avionics Laboratory, Wright-Patterson AFB, Ohio.

Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author)	2a. REPORT SECURITY CLASSIFICATION
Naval Research Laboratory Washington, D.C. 20390	Unclassified
	2b. GROUP

3. REPORT TITLE

COMPARATIVE ANALYSIS OF THE USE OF DYNAMIC AND STATIC SHIFT REGISTERS IN DIGITAL SIGNAL PROCESSORS

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)

An interim report on one phase of the NRL Problem.

5. AUTHOR(S) (First name, middle initial, last name)

Lawrence M. Leibowitz

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
December 26, 1972	20	2

8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
NRL Problem R02-46 b. PROJECT NO.	NRL Report 7482
c.	9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)
d.	

10. DISTRIBUTION STATEMENT

Distribution limited to U.S. Government Agencies only; test and evaluation; December 1972. Other requests for this document must be referred to the Director, Naval Research Laboratory, Washington, D.C. 20390.

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
	Department of the Navy Naval Air Systems Command Washington, D.C. 20360

13. ABSTRACT

High-density shift-register devices are used in many present-day data-processing systems such as radar digital signal processors. The number of bits of shift-register storage required increases with the need for greater radar range and resolution capability. The large-scale integrated (LSI) MOS circuit technology currently offers the possibility of shift registers of tens of thousands of bits per cubic inch with average power dissipation below 200 μW per bit. These units can be implemented for dynamic or static operation with inherent higher power dissipation in the latter case, due to the additional circuitry required. The key characteristics of these implementations are the need for continuous clocking above some minimum frequency in the dynamic case and negligible power dissipation during quiescent operation in the static case. This report analyzes the relative power dissipation of dynamic and static models of complimentary MOS (CMOS) shift registers as applied to a digital-feedback-integrator signal processor for the practical case of a nonunity processing duty factor.

The concepts of shift-register multiplexing and staggering for the purpose of power-dissipation reduction are described and extensively analyzed. It is shown that in practice the amount of reduction in dissipated power is limited by the power required by the additional circuitry used to achieve multiplexing or staggering. The relative power dissipation for each of the different configurations is derived for the dynamic- and static-register models. For the models considered, the static-register configurations dissipate less power than the dynamic-register configurations, due to the recirculation required in the dynamic case. An "extended register" technique, which reduces the power dissipation of the dynamic registers, is presented and analyzed.

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Shift registers						
Digital signal processing						
MOS technology						
Dynamic shift registers						
Static shift registers						
Digital feedback integrator						
CMOS technology						
Recirculation						
Serial register						
Multiplexed register						
Staggered register						
Extended register						
Processing duty factor						